

Exhibit 10

INTER PARTES REEXAMINATION COMMUNICATION	Control No. <i>195/001,339</i> <i>95/000,578 + 95/000,579</i>	Patent Under Reexamination	
	Examiner	7619912	
	WOO H. CHOI	Art Unit	
		3992	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address.* --

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS ACTION IS SET TO EXPIRE
 2 MONTH(S) THIRTY DAYS FROM THE MAILING DATE OF THIS LETTER. EXTENSIONS OF TIME FOR PATENT OWNER ARE GOVERNED BY 37 CFR 1.956.

Each time the patent owner responds to this Office action, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the Central Reexamination Unit at the mail, FAX, or hand-carry addresses given at the end of this Office action.

OFFICE ACTION IN INTER PARTES REEXAMINATION	Control No. <i>+95/001,339</i> 95/000,578 + 95/000,579	Patent Under Reexamination 7619912
	Examiner WOO H. CHOI	Art Unit 3992

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Responsive to the communication(s) filed by:

Patent Owner on 1/14/2012

Third Party(ies) on 2/13/2012, 3/30/2012, 2/23/2012

RESPONSE TIMES ARE SET TO EXPIRE AS FOLLOWS:

For Patent Owner's Response:

1 MONTH(S) from the mailing date of this action. 37 CFR 1.945. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.956.

For Third Party Requester's Comments on the Patent Owner Response:

30 DAYS from the date of service of any patent owner's response. 37 CFR 1.947. NO EXTENSIONS OF TIME ARE PERMITTED. 35 U.S.C. 314(b)(2).

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

This action is not an Action Closing Prosecution under 37 CFR 1.949, nor is it a Right of Appeal Notice under 37 CFR 1.953.

PART I. THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. Notice of References Cited by Examiner, PTO-892
2. Information Disclosure Citation, PTO/SB/08
3. _____

PART II. SUMMARY OF ACTION:

- 1a. Claims 1-136 are subject to reexamination.
- 1b. Claims _____ are not subject to reexamination.
2. Claims 64-66,94-108 and 112-118 have been canceled.
3. Claims _____ are confirmed. [Unamended patent claims]
4. Claims See Continuation Sheet are patentable. [Amended or new claims]
5. Claims See Continuation Sheet are rejected.
6. Claims _____ are objected to.
7. The drawings filed on _____ are acceptable are not acceptable.
8. The drawing correction request filed on _____ is: approved. disapproved.
9. Acknowledgment is made of the claim for priority under 35 U.S.C. 119 (a)-(d). The certified copy has: been received. not been received. been filed in Application/Control No 95000578.
10. Other _____

Continuation Sheet (PTOL-2064)

Control No. 95/000,578

Continuation of SUMMARY OF ACTION: 4. Claims patentable. [Amended or new claims] are 1,3,4,6,8,10-20,22,24,25,27-29,31,32,34-43,45-50,56,58,60-63,75-76,80,81,85,86,90-93,109-111 and 120-136.

Continuation of SUMMARY OF ACTION: 5. Claims rejected are 2,5-7,9,21,23,26,30,33,44,51-55,57,59,67-74,77-79,82-84,87-89 and 119.

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INTER PARTES REEXAMINATION OFFICE ACTION

1. This is an *inter partes* reexamination of U.S. Patent No. 7,619,912 ('912 patent). The following is a brief summary of the proceeding to date:

- 1) On June 8, 2010, a third party requester ("Requester 1") filed a request for inter partes reexamination of claims 1-51 of the '912 patent. The request was assigned the serial number 95/001,339 ("1339 Request").
- 2) On September 1, 2010, the Examiner issued an Order granting the reexamination. On the same day, the Examiner also issued an Action Closing Prosecution ("APC"), in which the Examiner did not adopt any of the proposed rejections and confirmed all claims over the prior art references applied in the proposed rejections.
- 3) On October 20, 2010, a second third party requester ("Requester 2") filed a request for reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50. The request was assigned the control number 95/000,578 ("578 Request").
- 4) On October 21, 2010, yet another third party requester ("Requester 3") filed a request for reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50. The request was assigned the control number 95/000,579 ("579 Request").
- 5) On January 14, 2011, an Order granting the reexamination requested by Requester 3 was mailed.
- 6) On January 18, 2011, an Order granting the reexamination requested by Requester 2 was mailed.

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least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for read or write access (all signals generations in a memory module are for read or write access).

49. With respect to claims 77, 82 and 87, see claim 67 above.

50. With respect to claim 78, 83 and 88, see claim 69 above.

51. With respect to claim 79, 84 and 89, see claim 68 above.

52. Proposed rejection of claims 1, 3-4, 6, 8, 10-20, 24-25, 27-29, 31-32, 34, 36-43, 45-48, 50, 55, 58-59, 75-76, 80-81, 85-86, 92-93, 120-126, 128-130, and 132-133 is not adopted.

53. With respect to claims 1, 3-4, 6, 8, 10-15, 18-20, 24-25, 27-29, 31-32, 34, 36-43, 45-48, 50, 75-76, 80-81, 85-86, 92-93, 120-126, 128-130, and 132-133, these claims recite the limitation “**wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals.**” As discussed above, Amidi does not teach generating CAS signals or chip select signal in response to a bank address signal.

54. With respect to claims 16 and 17, Requester 1 asserts that “[o]ne of ordinary skill in the art would have understood from the ‘152 publication that the command signal may be

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transmitted to the DDR memory devices serially in a sequential fashion” without any reasoned explanation to support the assertion. Conclusion of obviousness requires more than a mere conclusory statement. The claims require transmission of a command signal to only one DDR memory device at a time. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only one DDR memory device at a time when there is a plurality of memory devices in a rank.

55. With respect to claims 55 and 59, Amidi does not disclose transmitting and not transmitting a command signal to a plurality of memory devices.

56. With respect to claim 58, Amidi does not disclose **the generation of the first number of chip-select signals of the output control signals by the logic element is responsive at least in part to the bank address signals.**

Ground 5

57. Requester 1 asserts that claims 1-51 are obvious over Amidi in view of Dell 2. Proposed rejection of claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 44, and 51 is adopted. Proposed rejection of claims 1, 3-4, 6, 8, 10-20, 22, 24-25, 27-29, 31-32, 34-43, and 45-50 is not adopted.

58. Claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 44, and 51 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of Dell 2.

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59. With respect to claims 2, 5, 7, 9, 21, 23, 30, 33, 44, and 51, see Ground 3 above. Because these claims are anticipated by Amidi, they are obvious over Amidi and Dell 2

60. Proposed rejection of claims 1, 3-4, 6, 8, 10-20, 22, 24-25, 27-29, 31-32, 34-43, and 45-50 is not adopted.

61. With respect to claim claims 1, 3-4, 6, 8, 10-15, 18-20, 22, 24-25, 27-29, 31-32, 34-43, and 45-50, see the discussion of these claims above (Ground 3).

62. With respect to claims 16 and 17, see the discussion of these claims above (Ground 4).

Ground 6

63. Requester 2 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, 50, 52-75, and 77-136 are obvious over Amidi in view of JEDEC standards. Requester 1 asserts that claims 56, 60-63, 90-91, and 109-111 are obvious over Amidi in view of JEDEC standards. Proposed rejection of claims 7, 9, 21, 33, 44, 52-54, 57, 67-74, 77-79, 82-84, 87-89, and 119 is adopted. Proposed rejection of claims 1, 3-4, 6, 8, 10-11, 15, 18-20, 22, 24-25, 27-29, 31-32, 34, 36-39, 41-43, 45, 50, 55-56, 58-63, 75-76, 80-81, 85-86, 90-93, 109-111, and 120-136 is not adopted. Proposed rejection of claims 64-66, 94-108 and 112-118 is moot because they have been cancelled.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810
25224	7590	08/01/2013	EXAMINER	
MORRISON & FOERSTER, LLP			PEIKARI, BEHZAD	
707 Wilshire Boulevard			ART UNIT	
LOS ANGELES, CA 90017			3992	
			PAPER NUMBER	
			MAIL DATE	
			08/01/2013	
			DELIVERY MODE	
			PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Inter Partes Reexamination Control Nos.:
95/000,578; 95/000,579; 95/001,339
Attorney Docket No. 17730-3

I. INTRODUCTION

Third Party Requester SMART Modular Technology (WWH) Inc. (“SMART Modular”) submits these third party comments to the Office Action of November 13, 2012 and Patent Owner’s January 14, 2013 Response thereto.

SMART Modular respectfully disagrees with the Examiner’s statements of patentability, particularly over Ground 5: Amidi in view of Dell 2. The Examiner found that the majority of the allowed claims were patentable over Ground 5 because they require “the logic element generates gated column access strobe (CAS) signals or chip select signals in response at least in part to a bank address signal of the set of input control signals.” This limitation, however, is obvious under 35 U.S.C. § 103(a) over Amidi in view of Dell 2 because Dell 2 discloses the use of bank address signals by a logic element like the one disclosed in Amidi. Accordingly, for the reasons identified below, SMART Modular requests that the examiner reject the remaining uncanceled claims as obvious over Amidi in View of Dell 2.

SMART Modular also requests that the Examiner consider all pending claims as obvious under 35 U.S.C. § 103(a) over Amidi in view of U.S. Patent No. 6,446,184 (“Dell 184”). The Dell 184 reference first became known to SMART Modular after the filing of the request for *inter partes* reexamination and, therefore may be cited at this time. 37 C.F.R. § 1.948(a)(3); MPEP § 2666.05. Moreover, the combination of Amidi and Dell 184 renders obvious every pending claim as explained below. Accordingly, SMART Modular requests that the Examiner reject the remaining uncanceled claims as obvious over Amidi in View of Dell 184.

II. SMART MODULAR HAS NOT REQUESTED REEXAMINATION OF CLAIMS 2, 5, 12-14, 16-17, 23, 26, 30, 35, 40, 46-49, AND 51

SMART Modular has not requested reexamination of claims 2, 5, 12-14, 16-17, 23, 26, 30, 35, 40, 46-49, and 51 because Patent Owner has not asserted them against SMART Modular in litigation. Other requestors, however, have requested reexamination of those claims in this consolidated action, and the Examiner has addressed those claims in light of the prior art of record. SMART Modular responds to the Examiners statements for the benefit of a full record but it has not had an adequate opportunity to search for prior art addressing the limitations of those claims. Accordingly, SMART Modular reserves its right to argue invalidity of those claims in any future proceedings in which those arguments may become necessary.

III. THE EXAMINER SHOULD MAINTAIN ALL PENDING REJECTIONS

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b. Differences Between Claimed Invention and Amidi, And Resolution of Knowledge of One of Ordinary Skill In The Art

Please see above for the legal standard for obvious, the level of ordinary skill in the art, and for the motivation to combine.

Although the Examiner has found that Amidi does not explicitly disclose that the CPLD generates the chip-select signals “in response at least in part to a bank address signal of the set of input control signals,” this is disclosed by Dell 2. *See Claim 1.*

15. Claim 15

Amidi in view of Dell 2 renders claim 15 obvious under 35 U.S.C. § 103(a). Requestor provides a concise statement of the substantial new question of patentability for this claim based on Amidi in view of Dell 2 under 35 U.S.C. § 103.

a. Scope and Content of Amidi

In addition to the limitations of Claim 1, Claim 15 requires “the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks.” Amidi discloses the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks.

Amidi teaches that the CPLD and register respond to a command signal, such as the refresh or precharge signal, and the set of input control signals by generating and transmitting a second command signal to the appropriate rank of memory devices. For example, the CPLD generates transmits the Auto Precharge, Auto Refresh, and Load Mode Register commands according to the set of input control and command signals..

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CPLD 604 also ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank memory modules.
For example, CPLD 604 generates rcs2 and rcs3, besides rcs0 and rcs1 off of CS0, CS1 and Add(n) from the memory controller side. CPLD 604 also generates rcs2 when CS0 Auto Precharge all Banks Commands are issued. CPLD 604 also generates rcs3 when CS1 Auto Precharge all Banks Commands are issued. CPLD 604 also generates rcs2 when CS0 Auto Refresh Commands are issued. CPLD 604 also generates rcs3 when CS1 Auto Refresh Commands are issued. CPLD 604 also generates rcs2 when CS0 Load Mode Register Commands are issued. CPLD 604 also generates rcs3 when CS1 Load Mode Register Commands are issued.

Ex. PA-D, Amidi, ¶ 0052 (emphasis added).

b. Differences Between Claimed Invention and Amidi, And Resolution of Knowledge of One of Ordinary Skill In The Art

Please see above for the legal standard for obvious, the level of ordinary skill in the art, and for the motivation to combine.

Although the Examiner has found that Amidi does not explicitly disclose that the CPLD generates the chip-select signals “in response at least in part to a bank address signal of the set of input control signals,” this is disclosed by Dell 2. **See Claim 1.**

16. Claim 16

Amidi in view of Dell 2 renders claim 16 obvious under 35 U.S.C. § 103(a). Requestor provides a concise statement of the substantial new question of patentability for this claim based on Amidi in view of Dell 2 under 35 U.S.C. § 103.

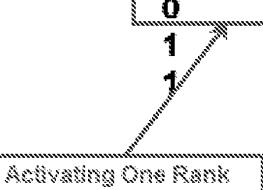
a. Scope and Content of Amidi

In addition to the limitations of Claim 15, Claim 16 requires “the command signal is transmitted to only one DDR memory device at a time.” To the extent the Examiner construes the limitation “the command signal is transmitted to only one DDR memory device at a time” as requiring only that the command signals are sent to a single rank because “one memory device” encompasses a rank of memory, Amidi discloses this limitation. Specifically, for one embodiment, Amidi discloses that the CPLD decodes two chip-select signals and a row address bit into three chip-select signals. **Ex. PA-D**, Amidi, ¶ 0044 and Figure 5. Using these three signals, the CPLD can activate each one of the four ranks of memory devices individually. *Id.*

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Add(n)	CS1	CS0	Active Bank
0	1	0	0
0	0	1	1
1	1	0	2
1	0	1	3

Activating One Rank



Id. When only one rank is selected, the command signal will be sent to only a single memory device based on the other address signals. **Ex. OTH-M**, Bagherzadeh Decl., ¶ 41.

b. Differences Between Claimed Invention and Amidi, And Resolution of Knowledge of One of Ordinary Skill In The Art

Please see above for the legal standard for obvious, the level of ordinary skill in the art, and for the motivation to combine.

Although the Examiner has found that Amidi does not explicitly disclose that the CPLD generates the chip-select signals “in response at least in part to a bank address signal of the set of input control signals,” this is disclosed by Dell 2. **See Claim 1.**

17. Claim 17

Amidi in view of Dell 2 renders claim 17 obvious under 35 U.S.C. § 103(a). Requestor provides a concise statement of the substantial new question of patentability for this claim based on Amidi in view of Dell 2 under 35 U.S.C. § 103.

a. Scope and Content of Amidi

In addition to the limitations of Claim 16, Claim 17 requires “the command signal comprises a read command.” Amidi discloses a memory module that uses read commands. Amidi discloses JEDEC compliant DIMMs. A person of ordinary skill in the art would understand that a READ command is one of the commands sent to the memory devices to initiate a read on an active row in a JEDEC compliant memory module. **Ex. OTH-M**, Bagherzadeh Decl., ¶ 43. This is disclosed by JEDEC 79-C at page 22, which a person of ordinary skill in the art would be aware of. *Id.*

b. Differences Between Claimed Invention and Amidi, And Resolution of Knowledge of One of Ordinary Skill In The Art